Implementation of 64-Bit Low Power Arithmetic Logic Unit using Multiplexers and Full adders for DSP Applications

Srinivasarao Alluri\textsuperscript{1}, M. V.Subbarao\textsuperscript{2}

\textsuperscript{1}Associate Professor Deparment of E.C.E, Tirumala Engineering College, A.P, India.
\textsuperscript{2}Assistant Professor, Dept. of E.C.E, Sri Vishnu Engineering College for Women, A.P, India.

Abstract: The main objective of this paper is to design low power 64-bit ALU. The proposed ALU is designed with the help of multiplexers and full adder. The main component in the ALU is full adder. In CMOS method eight transistor full adder and CMOS based multiplexers are used. In PTL method six transistor full adder and PTL based multiplexers are used. To reduce area, ripple carry adder is used in ALU. Pass transistor logic is used to reduce the number of transistors by eliminating redundant transistors. Number of active devices in PTL logic is less compared to CMOS logic. By using less number of active devices, power consumption is reduced. By reducing area and by using PTL based multiplexers low power ALU is attained. In the implementation of ALU using PTL method, the power and area are reduced to 55% compared to CMOS method.

Keywords: 6-Transistor Full Adder, 8-Transistor Full Adder, Arithmetic Logic Unit, CMOS Logic, Multiplexers, Pass Transistor Logic.

I. Introduction

The Arithmetic Logic Unit is essentially the heart of a CPU. It has more applications in DSP and micro-processors. In the past, VLSI designers concentrated more on area, performance, cost and reliability [1]. The least importance was given to power. Now a day’s power is given primary importance than area and speed. The two low power logic styles used in ALU are CMOS logic and PTL logic. Two important characteristics of CMOS logic are high noise immunity and low static power consumption. Since the one transistor of the complementary pair is always turned off. For high density logic functions CMOS logic is best. Pass transistor logic reduces transistor count by eliminating redundant transistors. By reducing transistors we can reduce area and then power. Here transistors are used as a switch to pass logic levels between nodes of a circuit, instead of connecting switches directly to supply voltages. This reduces number of active devices. With the increase in usage of portable devices, need for low power is increased greatly. Designers are always giving more importance to power rather than speed, because there is a reliability problem in high performance system. High performance systems often turns hot, and high temperature tends to exacerbate several silicon failure mechanisms. Every 10 degrees Celsius increase in operating temperature roughly doubles a component failure rate. From the environment point of view, the smaller the power dissipation of electronic systems, the lower the heat pumped into the rooms, the lower the electricity consumed and hence the lower the impact on global environment. There is always a tradeoff between power, area and delay. Depending upon requirement, the designer will selects the low power logic techniques.

II. ALU Design using CMOS Logic

The adder is one of the most important components of a CPU, Arithmetic logic unit (ALU) and address generation like cache. In addition, full-adders are important components in other applications such as digital signal processors (DSP) architectures and microprocessors. In the CMOS method 8-T full adder is used. Fig.1 shows the circuit level diagram of 8-T full adder [2]. Eight transistor Full adder is designed using two 3T XOR gates [5]. The Full adder inputs are three and the outputs of the Full adder are six namely, SUM, CARRY, AND, EXOR, EXNOR, OR. Additional OR circuit is used to perform OR operation. We can get EXNOR operation by giving output of EXOR to inverter circuit. Additional AND circuit was used to perform AND operation.

The multiplexers have been used in the ALU design for input and output signal selection. In CMOS method multiplexer is designed using CMOS logic. Inputs to 4:1 multiplexer are logic1, logic0, B0 and B0”. S0 and S1 are select signals. Depending upon select signals input will be selected as output. In CMOS method multiplexers are designed with the help of CMOS logic.

ALU is designed by using 4x1 multiplexer, 2x1 multiplexer and Full adder. The input and output sections consist of 4x1 and 2x1 multiplexers and the main logic is implemented by using full adder. In the first design multiplexers and full adder are implemented using the CMOS logic. A set of three select signals have been used in the design to determine the operation being performed and the inputs and outputs being selected. Fig. 2 shows the block diagram of 4-bit ALU [4]. Ripple carry adder is used in ALU. Here the carry bit cascaded from input to output stage [1]. The 4-bit ALU consists of eight 4x1 multiplexers, four 2x1 multiplexers and four full adders.
The 4-bit ALU is designed in 180nm, n-well CMOS technology. For the INCREMENT operation logic “0” is applied as an input. For DECREMENT operation logic 1 applied as input. The complement of B is used for SUBTRACTION operation. The full adder performs the SUBTRACT operation by two’s complement method. An INCREMENT operation is analyzed as adding “1” to the addend and DECREMENT is seen as a subtraction operation [4].

III. ALU Design using PTL

In PTL method Full adder is designed using six transistors. Six transistor Full adder is designed using 2T XOR gate [3]. In PTL method two transistor XOR gates can be designed using general logic implementation. The circuit operation is as follows when A=0 and B=0 both the PMOS transistors ON and it will produce the output low. When either one of the transistor is ON it produces output as high, when A=1 and B=1 both the PMOS transistors are OFF and it will produces output as low. The six transistor Full adder is shown in the Fig. 3 [3].

Fig. 3 Schematic of 6-T Full Adder

Here the multiplexer is implemented using pass transistors. This design is simple and efficient in terms of area and timing. The pass transistor design reduces the parasitic capacitances and results in fast circuits. There are two kinds of multiplexers implemented: 2 to 1 multiplexer and 4 to 1 multiplexer. Schematic of 4 to 1 Multiplexer and 2 to 1 Multiplexer is shown in the Fig. 4 [2] and Fig. 5 [2] respectively.
IV. Proposed Method for ALU Design

In Central Processing Unit (CPU) of a computer, Arithmetic and Logic Unit (ALU) is a fundamental building block and even the simplest microprocessors contain ALU. It is responsible for performing arithmetic as well as logical operations such as addition, subtraction, increment, decrement, logical AND, logical OR, logical XOR and logical XNOR. Eight 4x1 multiplexers, eight 2x1 multiplexers and four full adders are present in 4-bit ALU. The 4-bit ALU is designed in 250 nm, n-well CMOS technology. An INCREMENT and DECREMENT operations takes place when logic ‘1’ and logic ‘0’ are applied as an input. An INCREMENT operation is analyzed as adding ‘1’ to the addend and DECREMENT is seen as a subtraction operation [6]. For SUBTRACTION operation two’s complement method is used in which complement of \( B \) is used. The outputs obtained from the full adder are SUM, EXOR, EXNOR, AND & OR. Fig. 2 shows the 4-bit ALU where first stage to fourth stage is cascaded with the CARRY bit.

Based on the condition of the select signals, the multiplexer selects the appropriate input and gives it to the full adder which then computes the results. At the output of the multiplexer stage selects the appropriate output and route it to output port. Table 1 shows the truth table for the operations performed by the ALU based on the status of the select signal. The operation being performed and the inputs and outputs being selected are determined by set of three select signals incorporated in the design. Fig. 7 shows multiplexer logic at input port and Fig. 8 shows multiplexer logic at output port.

By using schematic editor of Tanner EDA the schematic of 4-bit ALU is designed. It shows connectivity between the components and describes aspect ratios of the transistor that can be modified along with the design. Fig. 9 represents the complete schematic view of ALU. The 4-bit ALU consists of two 4-bit inputs, three selecting lines, and one carry input, one carry output and four output bits.

<table>
<thead>
<tr>
<th>Selection Lines</th>
<th>Operations</th>
</tr>
</thead>
<tbody>
<tr>
<td>S2  S1  S0</td>
<td></td>
</tr>
<tr>
<td>0   0   0</td>
<td>AND</td>
</tr>
<tr>
<td>0   0   1</td>
<td>EXNOR</td>
</tr>
<tr>
<td>0   1   0</td>
<td>EXOR</td>
</tr>
<tr>
<td>0   1   1</td>
<td>OR</td>
</tr>
<tr>
<td>1   0   0</td>
<td>SUBTRACTION</td>
</tr>
<tr>
<td>1   0   1</td>
<td>INCREMENT</td>
</tr>
<tr>
<td>1   1   0</td>
<td>DECREMENT</td>
</tr>
<tr>
<td>1   1   1</td>
<td></td>
</tr>
</tbody>
</table>

Fig. 7 Multiplexer logic at the input stage

Fig. 8 Multiplexer logic at the output stage
Here ALU is designed using 6 transistor full adder and pass transistor logic based multiplexers. The pass transistor design reduces the parasitic capacitances and results in fast circuits. ALU operation depends upon select signals s0, s1 and s2. If s2=0 then it performs arithmetic operations. If s2=1 then it performs logical operations. The below Truth table gives the detailed explanation about ALU operation. Table 1 shows the Truth table of ALU. The Fig. 9 shows the schematic diagram of ALU. Tanner Tool is used to draw the schematic of 64 bit ALU.

V. Simulation Results

The simulation of ALU design is done using HSPICE. The technology file used is tsmc018. Full adder inputs are A, B, C and outputs are sum and carry.
PTL method is less than CMOS method. So area reduced and then power also reduced. As shown in tabular diagram the average power consumption in PTL method is around 55% less than CMOS method.

References


Author Profile

Srinivasarao Alluri received his BE degree from Andhra University, visakapatnam, India in 2004 and M.Tech from JNTU Hyderabad, India in 2012. Presently he is working as a Associate Professor, in Department of Electronics and Communication Engineering,Tirumala Engineering College, Guntur, A.P, India. His current areas of research interests include VLSI, Communication systems and Analog IC Design.

M. Venkata Subbarao received his B.Tech degree from JNTU, Hyderabad, India in 2008 and M.Tech from JNTU Kakinada, India in 2011. Presently he is working as a Assistant Professor, in Department of Electronics and Communication Engineering,Sri Vishnu Engineering College for women,Bhemavaram, A.P. His current areas of research interests include Signal Processing, Communication systems and Pattern Classification.